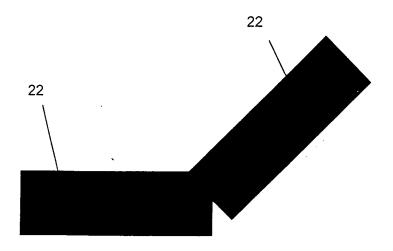
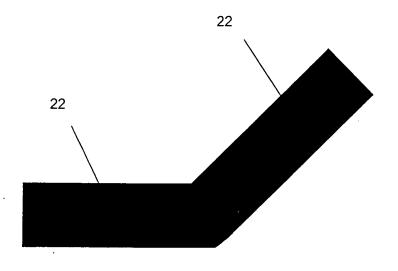


Figure 1 (PRIOR ART)



Before



After

Figure 1A (PRIOR ART)

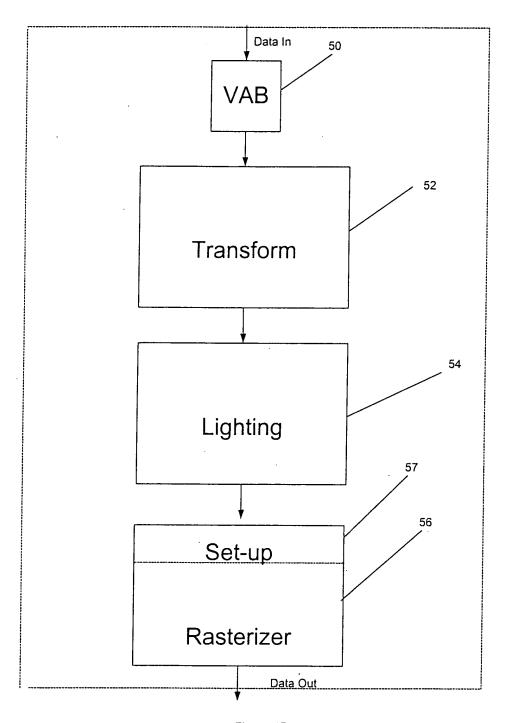


Figure 1B

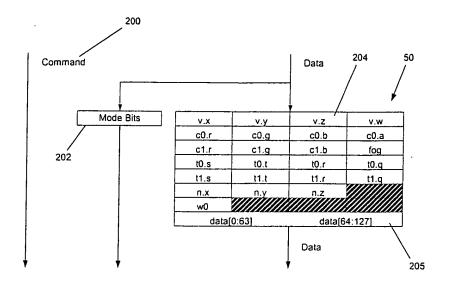
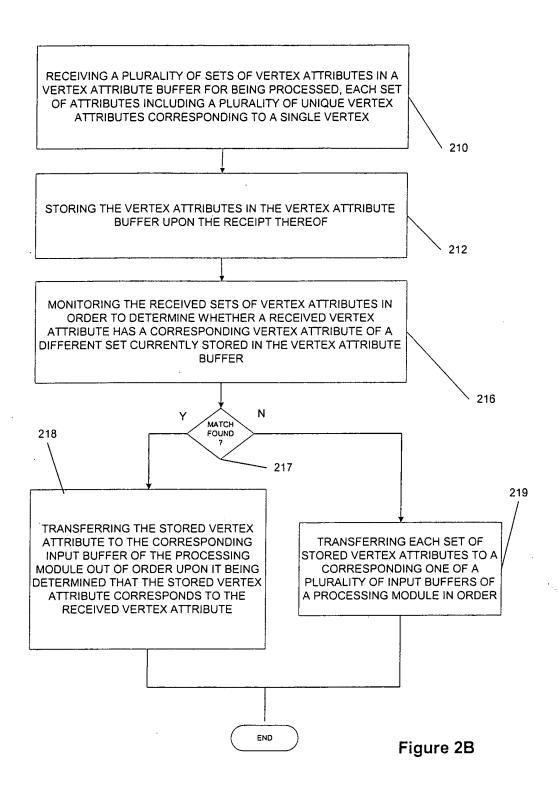


Figure 2

Command	Transform Stall	Lighting Stall	Description	
FE2XF_CMD_NOP			No operation. Can be used as a spacer between commands	
FE2XF_CMD_VERTEX	read	read	Vertex data.	
FE2XF_CMD_PASSTHR			Passthrough. Transform and lighting pass the data through.	
FE2XF_CMD_RDVAB			Read the VAB contents when context switching.	
FE2XF_CMD_LDMODE			Load new mode bits.	
FE2XF_CMD_LDXFCTX	write		Load transform context memory data	
FE2XF_CMD_RDXFCTX	read		Read transform context memory data.	
FE2XF_CMD_LDLTCTX		write	Load lighting context memory data.	
FE2XF_CMD_RDLTCTX		read	Read lighting context memory data.	
FE2XF_CMD_LDLTC0		write	Load lighting context0 memory data.	
FE2XF_CMD_RDLTC0		read	Read lighting context0 memory data.	
FE2XF_CMD_LDLTC1		write	Load lighting context1 memory data.	
FE2XF_CMD_RDLTC1		read	Read lighting context1 memory data.	
FE2XF_CMD_LDLTC2		write	Load lighting context2 memory data.	
FE2XF_CMD_RDLTC2		read	Read lighting context2 memory data.	
FE2XF_CMD_LTLTC3		write	Load lighting context3 memory data.	
FE2XF_CMD_RDLTC3		read	Read lighting context3 memory data.	
FE2XF_CMD_SYNC	read+write	read+write	Similar to NOP, but is not allowed to be processed in parallel.	

Figure 2A



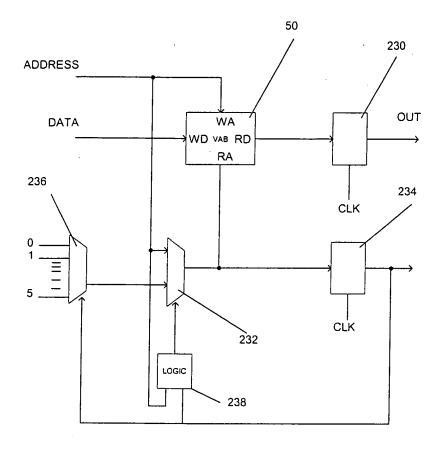


Figure 2C

N	Iode Bit	Bits	Description
T0		1	Texture 0 enable
TXF0		1	Texture 0 matrix transform enable
TDV0		1	Texture 0 w divide enable
T0S		3	Texture 0 texgen s control
TOT		3	Texture 0 texgen t control
TOU		3	Texture 0 texgen r control
T0Q		2	Texture 0 texgen q control
Tl		1	Texture I enable
TXFI		1	Texture 1 matrix transform enable
TDV!		1	Texture I w divide enable
TIS		3	Texture 1 texgen s control
TIT		3	Texture I texgen t control
TIU		3	Texture 1 texgen r control
TIQ		2	Texture 1 texgen q control
ETY		1	Eye type infinite(0) or local(1)
LIT		1	Lighting enable
NRM		1	Normal normalize enable
FOG		1	Fog enable
LIS		16	Light status (8 lights by 2 bits each,
			0:off,1:infinite,2:local, 3: spotlight)
FG	<u> </u>	2	Foggen control (0: off, 1: radial, 2: plane)
LAT		1	Light attenuation control (0: invert, 1: no invert)
CII	•	1	Specular color input enable
C10		1	Specular color output enable
CM	i	4	Color material control (1: emissive, 2:ambient, 4:
			diffuse, 8: specular)
PP		1	Point parameter enable
SKIN		1	Skinning enable
VPAS		1	Vertex pass enable

Figure 3

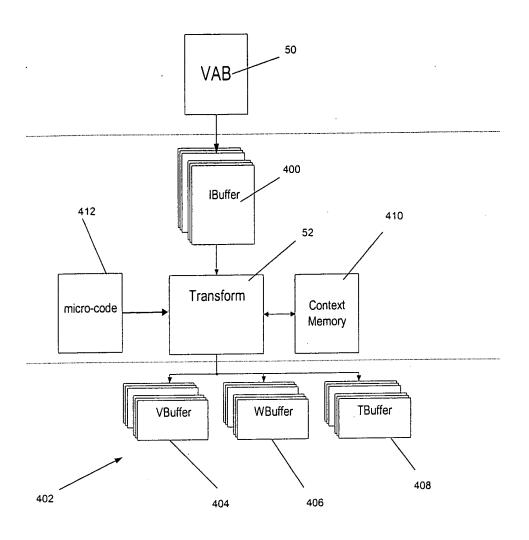


Figure 4

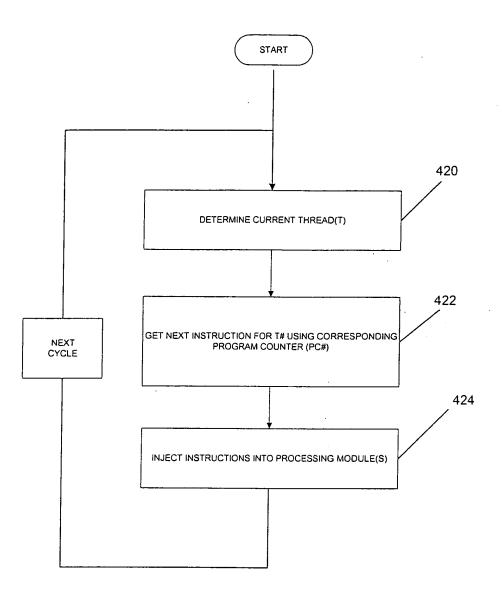


Figure 4A

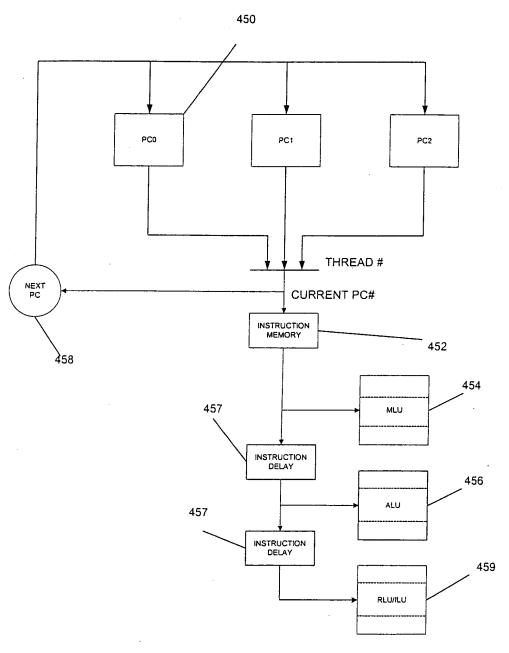
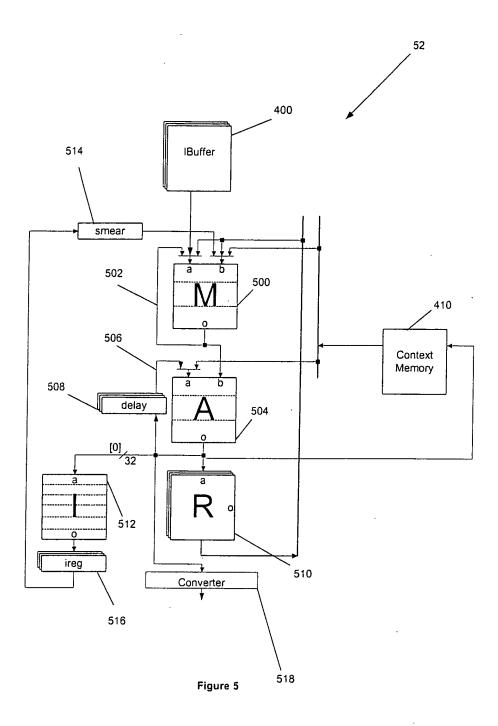
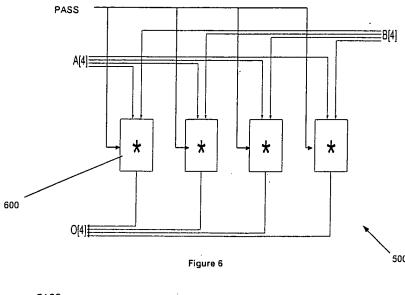


Figure 4B





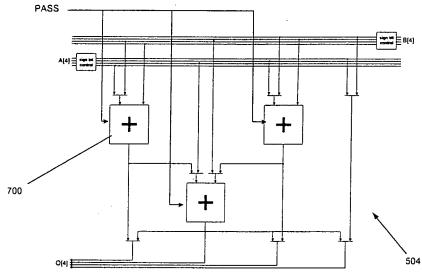


Figure 7

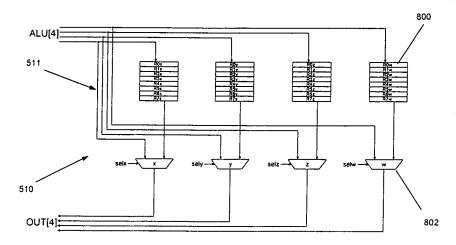


Figure 8

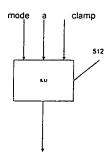


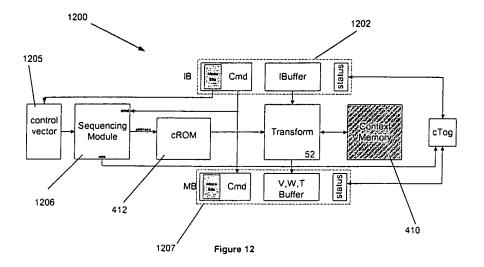
Figure 9

Address	Target	Action	Description
TPOS	TBUFFER	T[0] = ALU	Position
TT0	TBUFFER	T[3] = ALU	Texture0
TTI	TBUFFER	T[4] = ALU	Texture1
WEV	WBUFFER, VBUFFER	W[0] = ALU, V[0].y = ALU.w	Eye vector
WLV0	WBUFFER, VBUFFER	W[1] = ALU, V[1].y =	Light0 direction vector
WLVI	WBUFFER, VBUFFER	ALU.w W[2] = ALU, V[2].y = ALU.w	Light1 direction vector
WLV2	WBUFFER, VBUFFER	W[3] = ALU, V[3].y = ALU.w	Light2 direction vector
WLV3	WBUFFER, VBUFFER	W[4] = ALU, V[4].y = ALU.w	Light3 direction vector
WLV4	WBUFFER, VBUFFER	W[5] = ALU, V[5].y = ALU.w	Light4 direction vector
WLV5	WBUFFER, VBUFFER	W[6] = ALU, V[6].y = ALU.w	Light5 direction vector
WLV6	WBUFFER, VBUFFER	W[7] = ALU, V[7].y = ALU.w	Light6 direction vector
WLV7	WBUFFER, VBUFFER	W[8] = ALU, V[8].y = ALU.w	Light7 direction vector
WSL0	WBUFFER	W[9] = ALU	Spotlight0 cos
WSLI	WBUFFER	W[10] = ALU	Spotlight1 cos
WSL2	WBUFFER	W[11] = ALU	Spotlight2 cos
WSL3	WBUFFER	W[12] = ALU	Spotlight3 cos
WSL4	WBUFFER	W[13] = ALU	Spotlight4 cos
WSL5	WBUFFER	W[14] = ALU	Spotlight5 cos
WSL6	WBUFFER	W[15] = ALU	Spotlight6 cos
WSL7	WBUFFER	W[16] = ALU	Spotlight7 cos
VED	VBUFFER	V[0].x = 1.0, V[0].z = ALU.w	Eye radial distance vector
VLD0	VBUFFER	V[1].x = 1.0, V[1].z = ALU.w	Light0 distance vector
VLDI	VBUFFER	V[2].x = 1.0, V[2].z = ALU.w	Light 1 distance vector
VLD2	VBUFFER	V[3].x = 1.0, V[3].z = ALU.w	
VLD3	VBUFFER	V[4].x = 1.0, V[4].z = ALU.w	Light3 distance vector
VLD4	VBUFFER	V[5].x = 1.0, V[5].z = ALU.w	
VLD5	VBUFFER	V[6].x = 1.0, V[6].z = ALU.w	Light5 distance vector
VLD6	VBUFFER	V[7].x = 1.0, V[7].z = ALU.w	
VLD7	VBUFFER	V[8].x = 1.0, V[8].z = ALU.w	Light7 distance vector
VC0	VBUFFER,TBUFFER	V[9] = ALU, T[1] = ALU	Diffuse color
VC1	VBUFFER,TBUFFER	V[10] = ALU, T[2] = ALU	Specular color
VNRM	VBUFFER	V[11] = ALU	Normal vector
VED2	VBUFFER	V[12] = ALU	Eye planar distance vector
TVW_NOP			No valid output.

Figure 10

Microcode Field	Bits	Location	Delay	Description
oa	6	0: 5	2	Output buffer write address
гта	3	6: 8	0	RLU read address
rwm	4	9:12	2	RLU write mask
rwa	3	13:15	2	RLU write address
ilu	2	16:17	2	ILU operation
alu	4	18:21	1	ALU operation
ais	2	22:23	1	ALU sign control
aia	1	24	1	ALU input A mux
mlu	3	25:27	0	MLU operation
mib	2	28:29	0	MLU input B mux
mia	2	30:31	0	MLU input A mux
va	3	32:34	0	Input buffer read address
ce	1	35	0,2	Context memory read/write
ca	6	36:41	0,2	Context memory address
mr	2	42:43	0	MLU input vector rotate

Figure 11



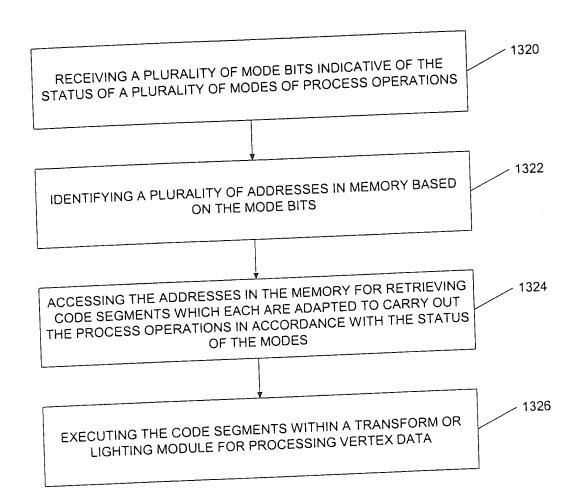


Figure 13

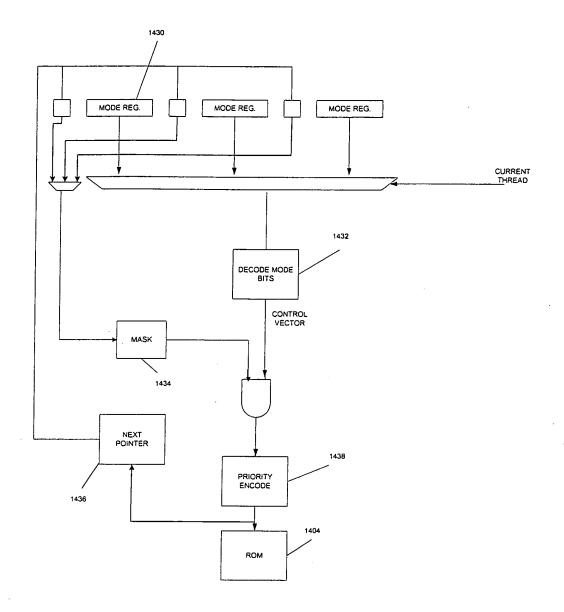


Figure 14

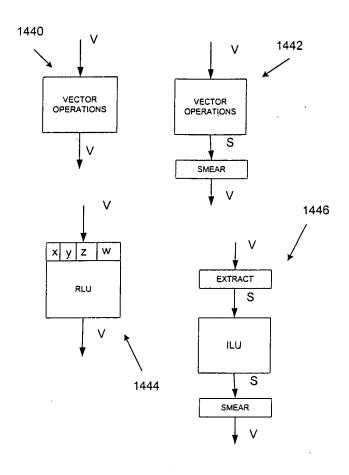


Figure 14A

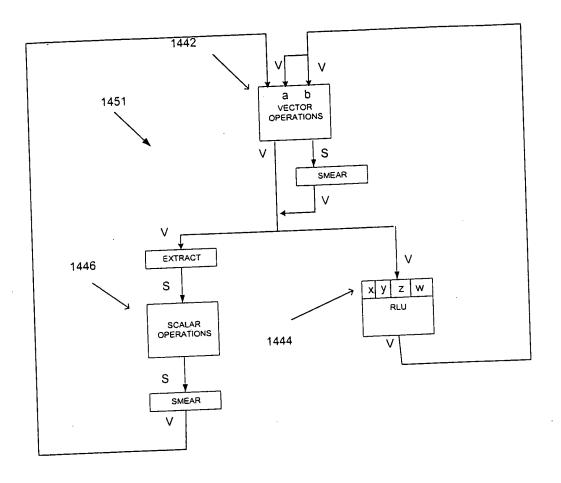


Figure 14B

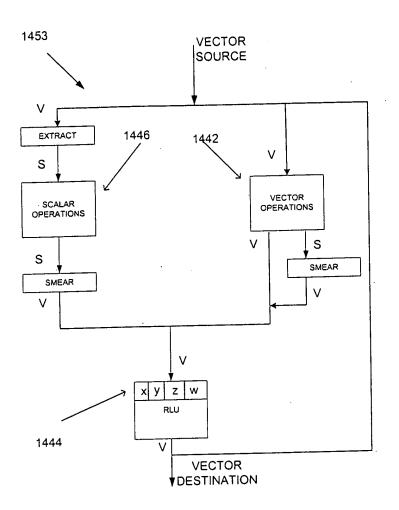


Figure 14C

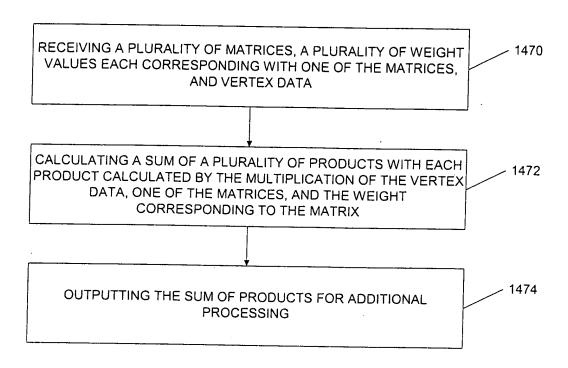


Figure 14D

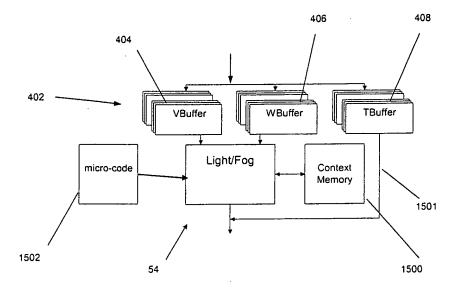
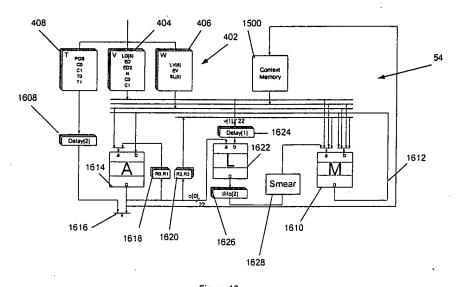
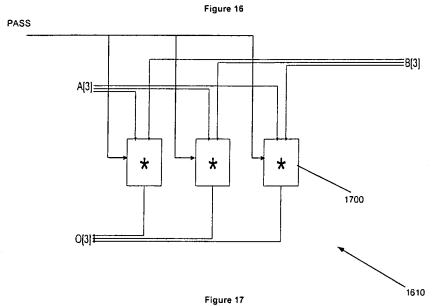
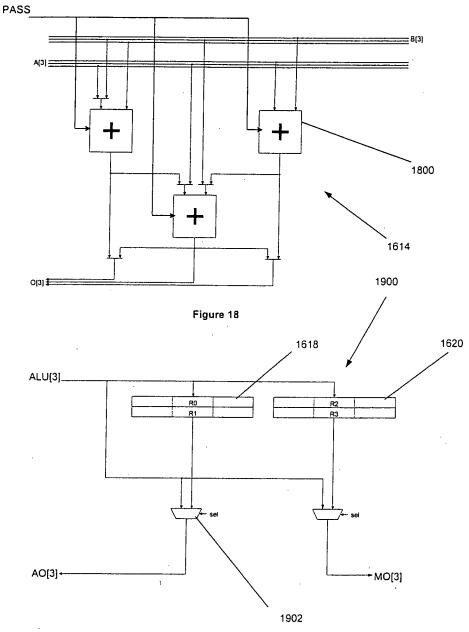
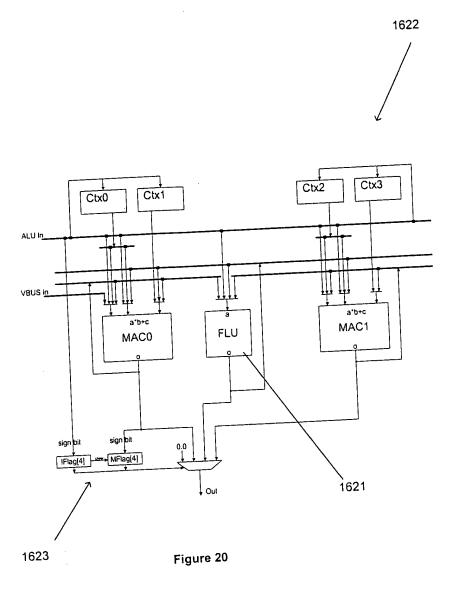


Figure 15







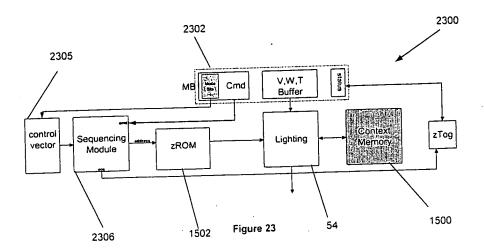


Name	Register	Description The LAG to 0
Z	IFLAG	Clear flag. Sets IFLAG and MFLAG to 0. Spotlight cone flag. Set if vertex is outside spotlight cone.
C	IFLAG	Spotlight cone flag. Set if vertex is dustice specular? flag. Set if specular contribution is negative.
S	IFLAG	Specular2 flag. Set it specular continuation to any
D	IFLAG	Diffuse flag. Set if diffuse term is negative.
	MFLAG	Spotlight cone attenuation flag. Set if spotlight cone attenuation contribution is negative.
U	MFLAG	Spotlight cone attenuation riag. Set it spotlight Specular flag. Set if specular contribution is negative.
T	MFLAG	Specular flag. Set if specular continuation is regular flag. Set if vertex is too far away from the light.
R	MFLAG	Range flag. Set if vertex is 100 far and 1 form and 5

Figure 21

Microcode Field	Bits 3	Location	Delay	Description
oa		1	2	Output address
rwe	1	3	2	RLU write enable
rwa	2	4: 5	2	RLU write address
R23	1	6	0	RLU(MLU) read address
R01	1	7	1	RLU(ALU) read address
aia	1	8	<u> </u>	ALU input A mux
alu	2	9:10	1	ALU operation
mib	2	11:12	0	MLU input B mux
mia	2	13:14	0	MLU input A mux
mlu	2	15:16	0	MLU operation
mwa	5	17:21	0	MLU WBUFFER read address
awa	5	22:26	1	ALU WBUFFER read address
va	4	27:30	0	VBUFFER read address
OS	2	31:32	2	LLU output address
frm	6	33:38	2	Flag register mask
mfe	1	39	2	MFLAG write enable
mfa	2	40:41	2	MFLAG write address
ife	1	42	2	IFLAG write enable
ifa	2	43:44	2	IFLAG write address
fia	2	45:46	2	FLU input A mux
flu	3	47:49	2	FLU operation
Mlc	1	50	2	MACI input C mux
М1ь	2	51:52	2	MAC1 input B mux
Mia	2	53:54	2	MACI input A mux
M0c	2	55:56	2	MAC0 input C mux
M0b	2	57:58	2	MAC0 input B mux
M0a	2	59:60	2	MAC0 input A mux
ce	3	61:63	0,2	Context memory read/write enable
a	6	64:69	0,2	Context memory address
C3a	4	70:73	2	Context3 memory address
C2a	4	74.77	2	Context2 memory address
Cla	5	78:82	2	Context1 memory address
C0a	2	83:84	2	Context0 memory address

Figure 22



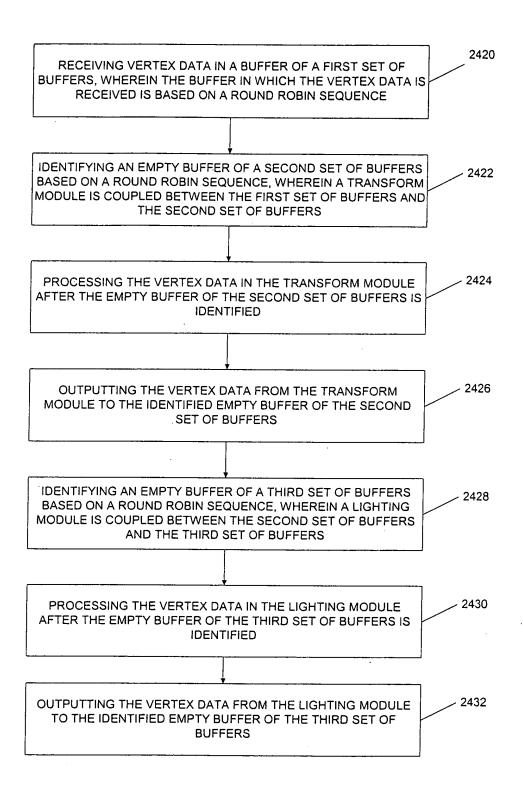


Figure 24

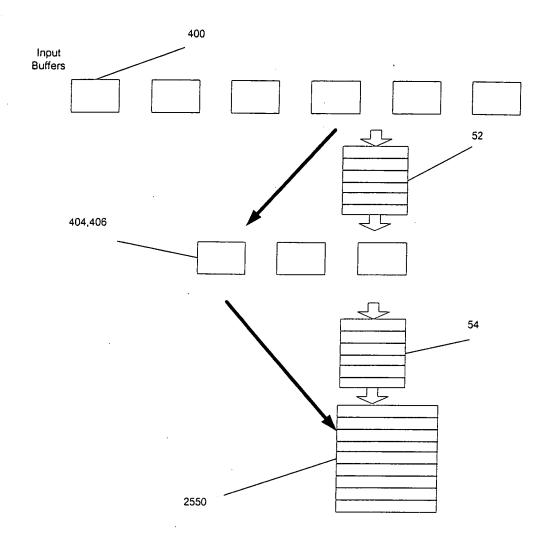


Figure 25

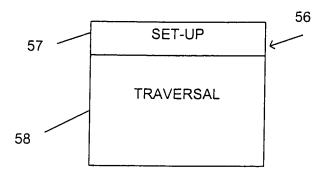


Figure 25B

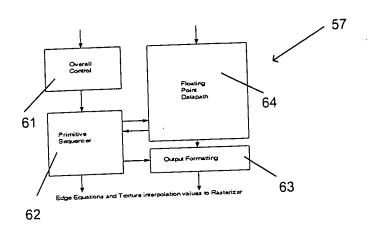


Figure 26

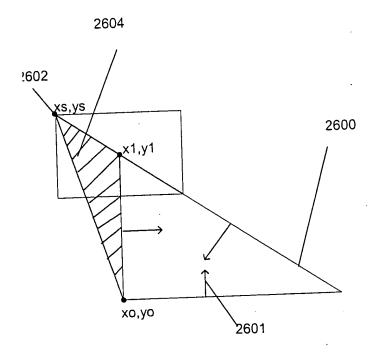


Figure 26A

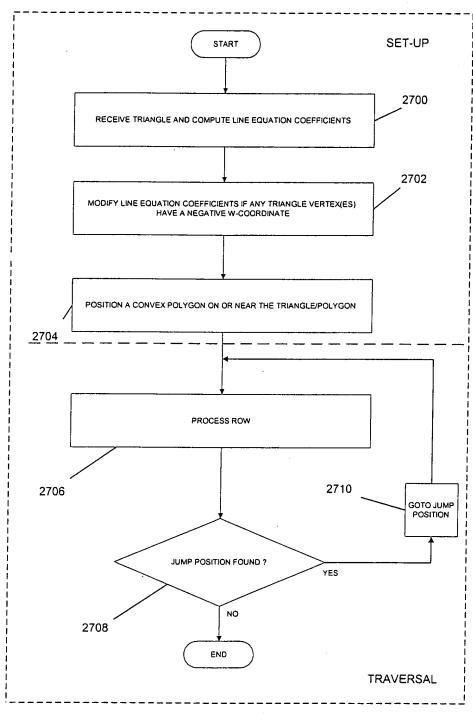


Figure 27

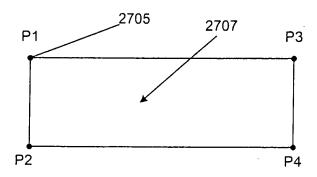
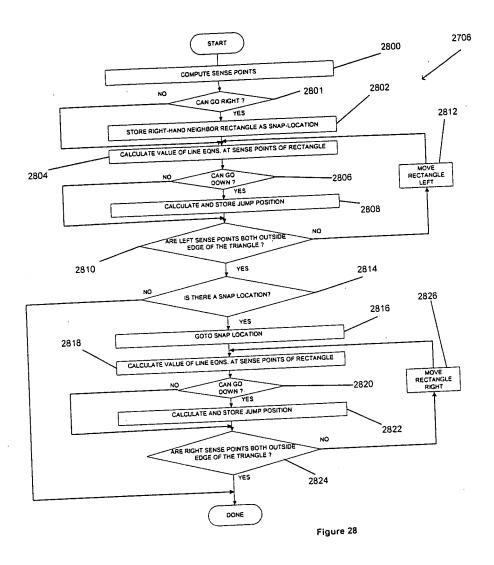


Figure 27A



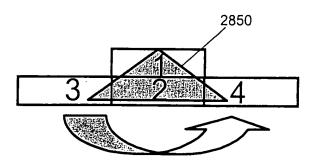


Figure 28A

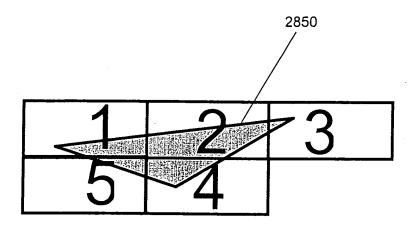


Figure 28B

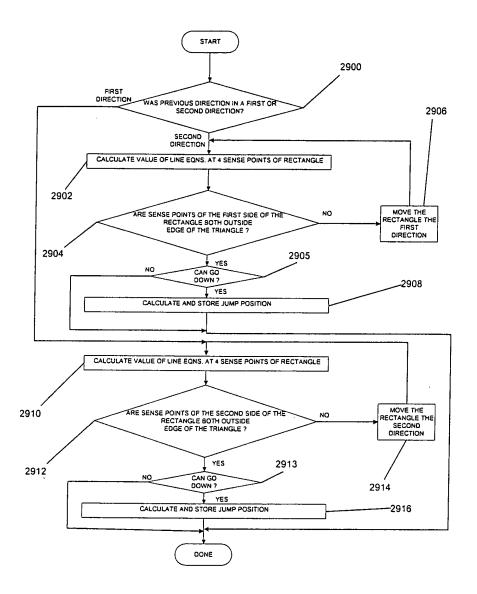
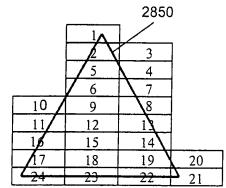
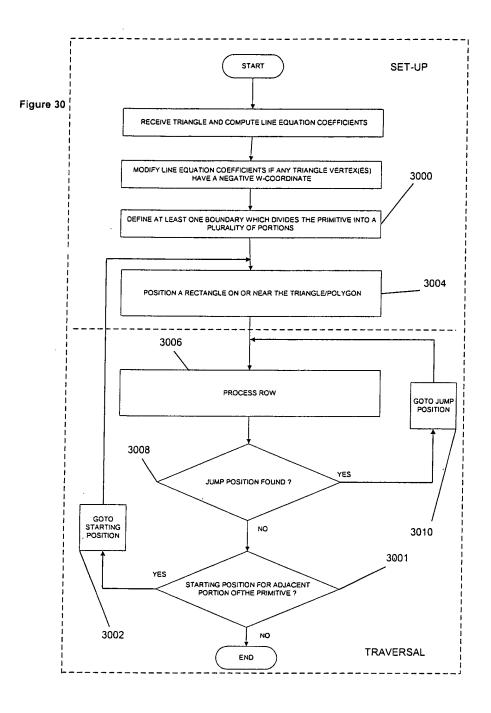


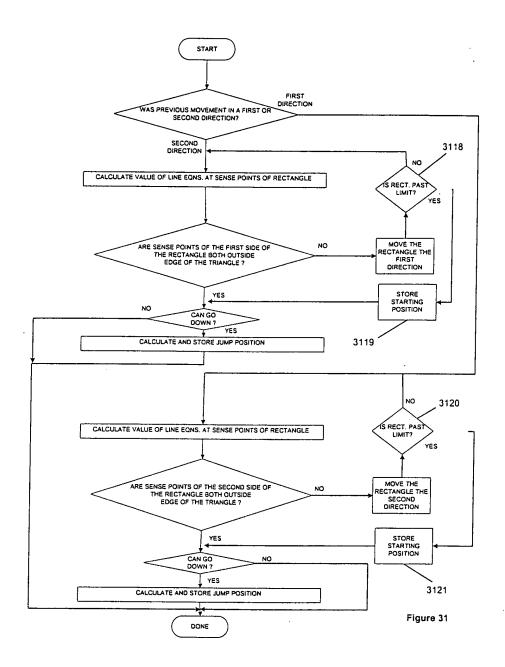
Figure 29

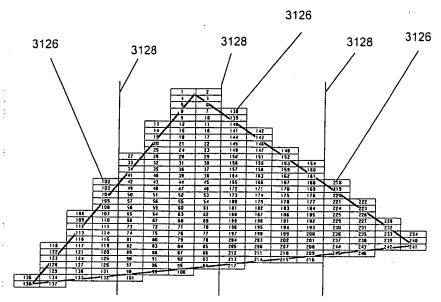


Boustrophedonic Footprint Sequence over a Triangle

Figure 29A







Swaths: 1-101, then 102-137, then 138-217, then 218-246

Figure 31A

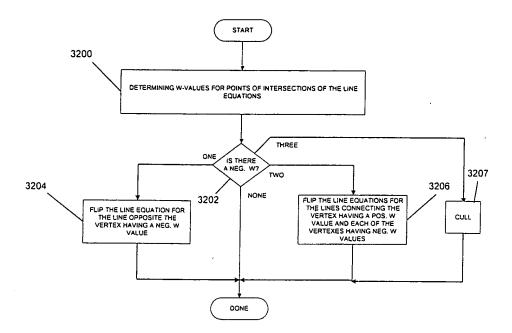


Figure 32

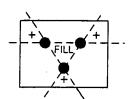


Figure 32A

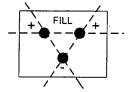


Figure 32B

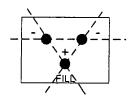


Figure 32C